

What is claimed is:

1. A data compression circuit in a memory device, comprising:
 - a first logic circuit for receiving data signals corresponding to a given bit location of each word of an output page of the memory device and for providing a first output signal indicative of whether each data signal has a first logic level;
 - a second logic circuit for receiving the data signals corresponding to the given bit location of each word of the output page of the memory device and for providing a second output signal indicative of whether each data signal has a second logic level different from the first logic level; and
 - a third logic circuit for receiving the first output signal and the second output signal and for providing a third output signal indicative of whether each data signal has the same logic level.
2. The data compression circuit of claim 1, wherein the first logic circuit further comprises:
 - a plurality of inputs, wherein the inputs are coupled to receive data signals corresponding to the given bit location of each word of the output page of the memory device; and
 - an output, wherein the output of the first logic circuit has a first logic level when each input receives a data signal having a logic low level and a second logic level when any input receives a data signal having a logic high level.
3. The data compression circuit of claim 2, wherein the first logic level of the first logic circuit is a logic high level and the second logic level of the first logic circuit is a logic low level.

4. The data compression circuit of claim 1, wherein the second logic circuit further comprises:
a plurality of inputs, wherein the inputs are coupled to receive data signals
corresponding to the given bit location of each word of the output page of
the memory device; and
an output, wherein the output of the second logic circuit has a first logic level when
each input receives a data signal having the logic high level and a second
logic level when any input receives a data signal having the logic low level.
5. The data compression circuit of claim 4, wherein the first logic level of the second
logic circuit is a logic low level and the second logic level of the second logic
circuit is a logic high level.
6. The data compression circuit of claim 1, wherein the first logic circuit is an OR
gate and the second logic circuit is an AND gate.
7. The data compression circuit of claim 1, wherein the first logic circuit is a NOR
gate and the second logic circuit is a NAND gate.
8. The data compression circuit of claim 1, wherein the third logic circuit is an XOR
gate.
9. The data compression circuit of claim 1, wherein the third logic circuit is an XNOR
gate.
10. A data compression circuit in a memory device, comprising:
a first logic circuit including a plurality of inputs coupled to receive data signals
corresponding to a given bit location of each word of an output page of the
memory device and further including an output for providing a first output
signal having a first output logic level when each input receives a data

signal having a first logic level and having a second output logic level when any input receives a data signal having a second logic level;

a second logic circuit including a plurality of inputs coupled to receive the data signals corresponding to the given bit location of each word of the output page of the memory device and further including an output for providing a second output signal having a first output logic level when each input receives a data signal having the second logic level and a second output logic level when any input receives a data signal having the first logic level; and

a third logic circuit coupled to receive the first output signal and the second output signal and to provide a third output signal indicative of whether each of the data signals has the same logic level.

11. The data compression circuit of claim 10, wherein the third logic circuit further comprises:
- a first input for receiving the first output signal;
 - a second input for receiving the second output signal; and
 - an output for providing the third output signal;
- wherein the third output signal has a first output logic level when the first output signal has its first output logic level;
- wherein the third output signal has its first logic level when the second output signal has its first output logic level; and
- wherein the third output signal has a second output logic level when the first output signal has its second output logic level and the second output signal has its second output logic level.
12. The data compression circuit of claim 10, wherein the first output logic level of the first output signal is different from the first output logic level of the second output signal.

13. The data compression circuit of claim 12, wherein the first output logic level of the first output signal is a logic high level, the second output logic level of the first output signal is a logic low level, the first output logic level of the second output signal is a logic low level and the second output logic level of the second output signal is a logic high level.
14. A data compression circuit in a memory device, comprising:
- a first logic circuit for receiving data signals corresponding to a given bit location of each word of an output page of the memory device and for providing a first output signal indicative of whether each data signal has a first logic level;
 - a second logic circuit for receiving the data signals corresponding to the given bit location of each word of the output page of the memory device and for providing a second output signal indicative of whether each data signal has a second logic level different from the first logic level; and
 - a third logic circuit for receiving the first output signal and the second output signal and for providing a third output signal indicative of whether each data signal has the same logic level;
- wherein the first logic circuit has a plurality of inputs and an output, wherein each input is coupled to receive a data signal corresponding to the given bit location of each word of the output page of the memory device in a one-to-one relationship, and wherein the output of the first logic circuit has a first logic level when each input receives a data signal having a logic low level and a second logic level when any input receives a data signal having a logic high level;
- wherein the second logic circuit has a plurality of inputs and an output, wherein each input is coupled to receive data signals corresponding to the given bit location of each word of the output page of the memory device in a one-to-one relationship, and wherein the output of the second logic circuit has a

first logic level when each input receives a data signal having the logic high level and a second logic level when any input receives a data signal having the logic low level;

wherein the third logic circuit has a first input for receiving the output of the first logic circuit, a second input for receiving the output of the second logic circuit, and an output;

wherein the output of the third logic circuit has a first logic level when the output of the first logic circuit has its first logic level;

wherein the output of the third logic circuit has its first logic level when the output of the second logic circuit has its first logic level; and

wherein the output of the third logic circuit has a second logic level when the output of the first logic circuit has its second logic level and the output of the second logic circuit has its second logic level.

15. A data compression circuit in a memory device, comprising:
- a first logic circuit for receiving data signals corresponding to a given bit location of each word of an output page of the memory device and for providing a first output signal indicative of whether each data signal has a first logic level;
 - a second logic circuit for receiving the data signals corresponding to the given bit location of each word of the output page of the memory device and for providing a second output signal indicative of whether each data signal has a second logic level different from the first logic level; and
 - a third logic circuit for receiving the first output signal and the second output signal and for providing a third output signal indicative of whether each data signal has the same logic level;
- wherein the first logic circuit further comprises a plurality of first buffer stages, each first buffer stage having an input for receiving a data signal for the given bit location of a word of the output page of the memory device and having an output, wherein each first buffer stage is coupled to receive a data

16. The data compression circuit of claim 15, wherein each first buffer stage sinks a first current level in response to a data signal having a logic high level and drives a second, larger, current level in response to a data signal having a logic low level.
17. The data compression circuit of claim 16, wherein the second current level for one first buffer stage is larger in magnitude than the first current level for each remaining first buffer stage combined.
18. The data compression circuit of claim 15, wherein each second buffer stage sinks a first current level in response to a data signal having a logic high level and drives a second, smaller, current level in response to a data signal having a logic low level.
19. The data compression circuit of claim 18, wherein the first current level for one second buffer stage is larger in magnitude than the second current level for each remaining second buffer stage combined.
20. The data compression circuit of claim 15, wherein each first buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one first buffer stage for each word of the output page.
21. The data compression circuit of claim 15, wherein each second buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one second buffer stage for each word of the output page.
22. The data compression circuit of claim 15, wherein each first buffer stage and each second buffer stage are further coupled to receive at least one control signal for selectively disabling the buffer stages.

23. The data compression circuit of claim 22, wherein each first buffer stage is a tri-state buffer circuit and the at least one control signal selectively tri-states each first buffer stage.
24. The data compression circuit of claim 22, wherein each second buffer stage is a tri-state buffer circuit and the at least one control signal selectively tri-states each second buffer stage.
25. A data compression circuit in a memory device, comprising:
a first logic circuit for receiving data signals corresponding to a given bit location of each word of an output page of the memory device and for providing a first output signal indicative of whether each data signal has a first logic level;
a second logic circuit for receiving the data signals corresponding to the given bit location of each word of the output page of the memory device and for providing a second output signal indicative of whether each data signal has a second logic level different from the first logic level; and
a third logic circuit for receiving the first output signal and the second output signal and for providing a third output signal indicative of whether each data signal has the same logic level;
wherein the first logic circuit further comprises a plurality of first buffer stages, each first buffer stage having an input coupled to receive a data signal for the given bit location of a word of the output page of the memory device and having an output, wherein the outputs of the first buffer stages are commonly coupled and wherein each first buffer stage further comprises:
a first p-channel field-effect transistor having a gate coupled to the input of its first buffer stage, a source coupled to a first potential node, and a drain coupled to the output of its first buffer stage; and

a first n-channel field-effect transistor having a gate coupled to the input of its first buffer stage, a source coupled to a second potential node, and a drain coupled to the output of its first buffer stage; wherein the first potential node is coupled to receive a first potential and the second potential node is coupled to receive a second potential lower than the first potential; and wherein the first p-channel field-effect transistor is sized to have a conductance at activation that is higher than a conductance at activation for the first n-channel field-effect transistor; wherein the second logic circuit further comprises a plurality of second buffer stages, each second buffer stage having an input coupled to receive a data signal for the given bit location of a word of the output page of the memory device and having an output, wherein the outputs of the second buffer stages are commonly coupled and wherein each second buffer stage further comprises:

a first p-channel field-effect transistor having a gate coupled to the input of its second buffer stage, a source coupled to a first potential node, and a drain coupled to the output of its second buffer stage; and a first n-channel field-effect transistor having a gate coupled to the input of its second buffer stage, a source coupled to a second potential node, and a drain coupled to the output of its second buffer stage; wherein the first potential node is coupled to receive a first potential and the second potential node is coupled to receive a second potential lower than the first potential; and wherein the first p-channel field-effect transistor is sized to have a conductance at activation that is lower than a conductance at activation for the first n-channel field-effect transistor; and wherein the third logic circuit further comprises a first input coupled to the commonly coupled outputs of the first buffer stages, a second input coupled to the commonly coupled outputs of the second buffer stages and an output,

wherein the output has a first logic level when logic levels received at the first and second inputs are the same and a second logic level when logic levels received at the first and second inputs differ.

26. The data compression circuit of claim 25, wherein the first p-channel field-effect transistor of a first buffer stage has a larger W/L ratio than the first n-channel field-effect transistor of the first buffer stage.
27. The data compression circuit of claim 26, wherein the first p-channel field-effect transistor of the first buffer stage has a W/L ratio of approximately 40/1 and the first n-channel field-effect transistor of the first buffer stage has a W/L ratio of approximately 3/10.
28. The data compression circuit of claim 25, wherein the first p-channel field-effect transistor of a second buffer stage has a smaller W/L ratio than the first n-channel field-effect transistor of the second buffer stage.
29. The data compression circuit of claim 28, wherein the first p-channel field-effect transistor of the second buffer stage has a W/L ratio of approximately 4/5 and the first n-channel field-effect transistor of the second buffer stage has a W/L ratio of approximately 20/1.
30. The data compression circuit of claim 25, wherein each first buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one first buffer stage for each word of the output page.
31. The data compression circuit of claim 25, wherein each second buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one second buffer stage for each word of the output page.

32. The data compression circuit of claim 25, wherein the first potential node of a first buffer stage is coupled to receive a supply potential.
33. The data compression circuit of claim 25, wherein the second potential node of a first buffer stage is coupled to receive a ground potential.
34. The data compression circuit of claim 25, wherein the first potential node of a second buffer stage is coupled to receive a supply potential.
35. The data compression circuit of claim 25, wherein the second potential node of a second buffer stage is coupled to receive a ground potential.
36. The data compression circuit of claim 25, wherein the first potential node of each first buffer stage and the first potential node of each second buffer stage are each coupled to receive the same supply potential.
37. The data compression circuit of claim 25, wherein the second potential node of each first buffer stage and the second potential node of each second buffer stage are each coupled to receive the same ground potential.
38. The data compression circuit of claim 25, further comprising:
wherein each first buffer stage further comprises a second p-channel field-effect transistor coupled between the first potential node and the first p-channel field-effect transistor and a second n-channel field-effect transistor coupled between the second potential node and the first n-channel field-effect transistor;
wherein the second p-channel field-effect transistor has a gate coupled to receive a first enable signal; and
wherein the second n-channel field-effect transistor has a gate coupled to receive a second enable signal different from the first enable signal.

39. The data compression circuit of claim 38, wherein the second enable signal is the binary complement of the first enable signal.
40. The data compression circuit of claim 25, further comprising:
wherein each second buffer stage further comprises a second p-channel field-effect transistor coupled between the first potential node and the first p-channel field-effect transistor and a second n-channel field-effect transistor coupled between the second potential node and the first n-channel field-effect transistor;
wherein the second p-channel field-effect transistor has a gate coupled to receive a first enable signal; and
wherein the second n-channel field-effect transistor has a gate coupled to receive a second enable signal different from the first enable signal.
41. The data compression circuit of claim 40, wherein the second enable signal is the binary complement of the first enable signal.
42. A memory device, comprising:
a data compression circuit having a plurality of inputs for receiving data signals and an output for providing a first control signal, wherein the data compression circuit has its inputs coupled to receive data signals representative of data values for a given bit location of each word of a page of output of the memory device, and wherein the first control signal has a first logic level when the data signals for the given bit location match and a second logic level when any data signal for the given bit location differs; and
an output driver circuit for providing an output signal indicative of a data signal, wherein the output driver circuit is disabled when the first control signal has the second logic level.

43. The memory device of claim 42, wherein the output driver circuit is responsive to a second control signal and its data signal when the first control signal has the first logic level.
44. The memory device of claim 43, wherein the second control signal is a global output enable signal.
45. The memory device of claim 43, wherein the first control signal and the second control signal are combined as part of a global inhibit signal and the output driver circuit is responsive to the global inhibit signal.
46. The memory device of claim 42, wherein the data compression circuit comprises:
a first logic circuit for receiving the data signals corresponding to the given bit location of each word of the output page of the memory device and for providing a first output signal indicative of whether each data signal has a first logic level;
a second logic circuit for receiving the data signals corresponding to the given bit location of each word of the output page of the memory device and for providing a second output signal indicative of whether each data signal has a second logic level different from the first logic level; and
a third logic circuit for receiving the first output signal and the second output signal and for providing the first control signal indicative of whether each data signal has the same logic level.
47. The memory device of claim 42, wherein the data compression circuit comprises:
a first logic circuit comprising:
a plurality of inputs, wherein the inputs are coupled to receive the data signals corresponding to the given bit location of each word of the output page of the memory device; and

an output, wherein the output of the first logic circuit has a first logic level when each input receives a data signal having a logic low level and a second logic level when any input receives a data signal having a logic high level;

a second logic circuit comprising:

a plurality of inputs, wherein the inputs are coupled to receive the data signals corresponding to the given bit location of each word of the output page of the memory device; and

an output, wherein the output of the second logic circuit has a first logic level when each input receives a data signal having the logic high level and a second logic level when any input receives a data signal having the logic low level; and

a third logic circuit comprising:

a first input for receiving the output of the first logic circuit;

a second input for receiving the output of the second logic circuit; and

an output for providing the first control signal;

wherein the first control signal has its first logic level when the output of the first logic circuit has its first logic level;

wherein first control signal has its first logic level when the output of the second logic circuit has its first logic level; and

wherein the first control signal has its second logic level when the output of the first logic circuit has its second logic level and the output of the second logic circuit has its second logic level.

48. The memory device of claim 47, wherein the first logic level of the first logic circuit is different from the first logic level of the second logic circuit.
49. The memory device of claim 48, wherein the first logic level of the first logic circuit is a logic high level, the second logic level of the first logic circuit is a logic

low level, the first logic level of the second logic circuit is a logic low level and the second logic level of the second logic circuit is a logic high level.

50. The memory device of claim 42, wherein the data compression circuit comprises:
- a plurality of first buffer stages, each first buffer stage having an input coupled to receive a data signal for the given bit location of a word of the output page of the memory device and having an output, wherein the outputs of the first buffer stages are commonly coupled and wherein each first buffer stage further comprises:
 - a first p-channel field-effect transistor having a gate coupled to the input of its first buffer stage, a source coupled to a first potential node, and a drain coupled to the output of its first buffer stage; and
 - a first n-channel field-effect transistor having a gate coupled to the input of its first buffer stage, a source coupled to a second potential node, and a drain coupled to the output of its first buffer stage;
 - wherein the first potential node is coupled to receive a first potential and the second potential node is coupled to receive a second potential lower than the first potential; and
 - wherein the first p-channel field-effect transistor is sized to have a conductance at activation that is higher than a conductance at activation for the first n-channel field-effect transistor;
 - a plurality of second buffer stages, each second buffer stage having an input coupled to receive a data signal for the given bit location of a word of the output page of the memory device and having an output, wherein the outputs of the second buffer stages are commonly coupled and wherein each second buffer stage further comprises:
 - a first p-channel field-effect transistor having a gate coupled to the input of its second buffer stage, a source coupled to a first potential node, and a drain coupled to the output of its second buffer stage; and

54. The memory device of claim 53, wherein the first p-channel field-effect transistor of the second buffer stage has a W/L ratio of approximately 4/5 and the first n-channel field-effect transistor of the second buffer stage has a W/L ratio of approximately 20/1.
55. The memory device of claim 50, wherein each first buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one first buffer stage for each word of the output page.
56. The memory device of claim 50, wherein each second buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one second buffer stage for each word of the output page.
57. The memory device of claim 50, wherein the first potential node of each first buffer stage and the first potential node of each second buffer stage are each coupled to receive the same supply potential.
58. The memory device of claim 50, wherein the second potential node of each first buffer stage and the second potential node of each second buffer stage are each coupled to receive the same ground potential.
59. The memory device of claim 50, further comprising:
wherein each first buffer stage further comprises a second p-channel field-effect transistor coupled between the first potential node and the first p-channel field-effect transistor and a second n-channel field-effect transistor coupled between the second potential node and the first n-channel field-effect transistor;
wherein the second p-channel field-effect transistor has a gate coupled to receive a first enable signal; and

wherein the second n-channel field-effect transistor has a gate coupled to receive a second enable signal different from the first enable signal.

60. The memory device of claim 59, wherein the second enable signal is the binary complement of the first enable signal.
61. The memory device of claim 50, further comprising:
wherein each second buffer stage further comprises a second p-channel field-effect transistor coupled between the first potential node and the first p-channel field-effect transistor and a second n-channel field-effect transistor coupled between the second potential node and the first n-channel field-effect transistor;
wherein the second p-channel field-effect transistor has a gate coupled to receive a first enable signal; and
wherein the second n-channel field-effect transistor has a gate coupled to receive a second enable signal different from the first enable signal.
62. The memory device of claim 61, wherein the second enable signal is the binary complement of the first enable signal.
63. The memory device of claim 42, wherein the memory device is coupled to a processor.
64. A memory device, comprising:
a first data compression circuit having a plurality of inputs for receiving data signals and an output for providing a first control signal, wherein the data compression circuit has its inputs coupled to receive data signals representative of data values for a given bit location of each word of a page of output of the memory device, and wherein the first control signal has a

first logic level when the data signals for the given bit location match and a second logic level when any data signal for the given bit location differs; an second data compression circuit having a plurality of inputs for receiving data signals and an output for providing a second control signal, wherein the second data compression circuit has its inputs coupled to receive data signals representative of data values for a different given bit location of each word of the page of output of the memory device, and wherein the second control signal has a first logic level when the data signals for the different given bit location match and a second logic level when any data signal for the different given bit location differs; a first output driver circuit for providing an output signal indicative of a data signal, wherein the first output driver circuit is disabled when the first control signal has the second logic level; and a second output driver circuit for providing an output signal indicative of a data signal, wherein the second output driver circuit is disabled when the second control signal has the second logic level.

65. The memory device of claim 64, wherein the additional output driver circuit is responsive to the second control signal and its data signal when a third control signal has the first logic level.
66. The memory device of claim 65, wherein the second output driver circuit is disabled when either the second control signal or the third control signal has its second logic level.
67. The memory device of claim 64, wherein the first control signal and a third control signal are combined as part of a global inhibit signal and each output driver circuit is responsive to the global inhibit signal.

68. The memory device of claim 64, wherein the control signal from each data compression circuit and a third control signal are ORed to generate a combined control signal, and wherein each output driver circuit is responsive to the combined control signal.
69. The memory device of claim 64, wherein each output driver circuit is disabled if any control signal of a data compression circuit is indicative of a mismatch between a data value for a bit location of a first word of the output page and data value for its corresponding bit location of any remaining word of the output page.
70. The memory device of claim 64, further comprising one data compression circuit and one output driver circuit corresponding to each bit location of a word of the output page of the memory device.
71. A memory device, comprising:
a data compression circuit having a plurality of inputs for receiving data signals and an output for providing a first control signal, wherein the data compression circuit has its inputs coupled to receive data signals representative of data values for a given bit location of each word of a page of output of the memory device, and wherein the first control signal has a first logic level when the data signals for the given bit location match and a second logic level when any data signal for the given bit location differs; and
an output driver circuit for providing an output signal indicative of a data signal, wherein the output driver circuit is disabled when the first control signal has the second logic level;
wherein the data compression circuit further comprises:
a plurality of first buffer stages, each first buffer stage having an input for receiving a data signal for the given bit location of a word of the output page of the memory device and having an output, wherein each first buffer stage is coupled to receive a data signal for the

given bit location of a different word of the output page and wherein each first buffer stage has its output coupled to the outputs of the remaining first buffer stages;

a plurality of second buffer stages, each second buffer stage having an input for receiving a data signal for the given bit location of a word of the output page of the memory device and having an output, wherein each second buffer stage is coupled to receive a data signal for the given bit location of a different word of the output page and wherein each second buffer stage has its output coupled to the outputs of the remaining second buffer stages; and

a logic circuit having a first input coupled to the outputs of the first buffer stages, a second input coupled to the outputs of the second buffer stages, and an output for providing the first control signal;

wherein the first input of the logic circuit has a first logic level when the data signal for the given bit location of each word of the output page has a logic low level and the first input of the logic circuit has a second logic level when the data signal for the given bit location of any word of the output page has a logic high level;

wherein the second input of the logic circuit has a first logic level when the data signal for the given bit location of each word of the output page has a logic high level and the second input of the logic circuit has a second logic level when the data signal for the given bit location of any word of the output page has a logic low level;

wherein the first control signal has its first logic level when the first input of the logic circuit has its first logic level;

wherein the first control signal has its first logic level when the second input of the logic circuit has its first logic level; and

wherein the first control signal has its second logic level when the first input of the logic circuit and the second input of the logic circuit each have their second logic levels.

72. The memory device of claim 71, wherein each first buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one first buffer stage for each word of the output page.
73. The memory device of claim 71, wherein each second buffer stage is coupled to receive a data signal corresponding to a different word of the output page and wherein there is one second buffer stage for each word of the output page.
74. The memory device of claim 71, wherein each first buffer stage and each second buffer stage are further coupled to receive at least one control signal for selectively disabling the buffer stages.
75. The memory device of claim 71, wherein each first buffer stage sinks a first current level in response to a data signal having a logic high level and drives a second, larger, current level in response to a data signal having a logic low level.
76. The memory device of claim 75, wherein the second current level for one first buffer stage is larger in magnitude than the first current level for each remaining first buffer stage combined.
77. The memory device of claim 71, wherein each second buffer stage sinks a first current level in response to a data signal having a logic high level and drives a second, smaller, current level in response to a data signal having a logic low level.
78. The memory device of claim 77, wherein the first current level for one second buffer stage is larger in magnitude than the second current level for each remaining second buffer stage combined.

79. A method of testing a memory device, comprising:
accessing a memory array to generate a page of output containing at least two words, wherein the page of output has a repeating data pattern and each word has at least one bit location;
comparing data signals for a given bit location of each word of the page of output;
disabling output for data signals corresponding to at least the given bit location if at least one data signal for the given bit location differs from any remaining data signal for the given bit location;
attempting to read a word of the page of output; and
determining whether output is disabled for at least the given bit location, wherein disabled output is indicative of failure of the memory device.
80. The method of claim 79, wherein attempting to read a word of the page of output comprises attempting to read only one word of the page of output.
81. The method of claim 79, further comprising:
writing the repeating data pattern to the memory array prior to accessing the memory array.
82. The method of claim 81, wherein the repeating data pattern is a repeating pattern of all zeros.
83. The method of claim 81, wherein the repeating data pattern is a repeating pattern of all ones.
84. The method of claim 81, wherein the repeating data pattern is a checkerboard pattern.
85. The method of claim 81, wherein the repeating data pattern is a reverse checkerboard pattern.

86. The method of claim 79, further comprising:
repeating the method for each page of output of the memory device.
87. The method of claim 79, wherein further comprising:
repeating the method for each page of output of the memory device and attempting
to read only one word of each page of output.
88. A method of testing a memory device, comprising:
accessing a memory array to generate a page of output containing at least two
words, wherein the page of output has a repeating data pattern and each
word has at least one bit location;
comparing data signals for a given bit location of each word of the page of output;
disabling output for data signals corresponding to at least the given bit location if at
least one data signal for the given bit location differs from any remaining
data signal for the given bit location;
attempting to read a word of the page of output;
determining whether output is disabled for at least the given bit location, wherein
disabled output is indicative of failure of the memory device;
comparing data signals for an additional given bit location of each word of the page
of output concurrently with comparing data signals for the given bit
location; and
disabling output for data signals corresponding to at least the additional given bit
location if at least one data signal for the additional given bit location
differs from any remaining data signal for the additional given bit location.
89. A method of testing a memory device, comprising:
accessing a memory array to generate a page of output containing at least two
words, wherein the page of output has a repeating data pattern and each
word has at least one bit location;

comparing data signals for a given bit location of each word of the page of output;
disabling output for data signals corresponding to at least the given bit location if at
least one data signal for the given bit location differs from any remaining
data signal for the given bit location;
attempting to read a word of the page of output;
determining whether output is disabled for at least the given bit location, wherein
disabled output is indicative of failure of the memory device;
comparing data signals for an additional given bit location of each word of the page
of output concurrently with comparing data signals for the given bit
location;
disabling output for all data signals if at least one data signal for the given bit
location differs from any remaining data signal for the given bit location;
and
disabling output for all data signals if at least one data signal for the additional
given bit location differs from any remaining data signal for the additional
given bit location.

90. The method of claim 89, wherein disabling output further comprises disabling an output driver circuit.
91. The method of claim 90, wherein disabling an output driver circuit further comprises tri-stating the output driver circuit.
92. The method of claim 89, wherein comparing data signals for a given bit location of each word of the page of output comprises applying the data signals to a first logic circuit and a second logic circuit, wherein the first logic circuit is configured to provide a first output signal indicative of whether each data signal has a first logic level, and wherein the second logic circuit is configured to provide a second output signal indicative of whether each data signal has a second logic level different from the first logic level.

93. The method of claim 92, wherein comparing data signals for a given bit location of each word of the page of output further comprises generating a control signal from the first output signal and the second output signal indicative of whether each data signal has the same logic level.
94. A method of testing a memory device, comprising:
accessing a memory array to generate a page of output containing at least two words, wherein the page of output has a repeating data pattern and each word has at least one bit location;
comparing data signals for a given bit location of each word of the page of output;
disabling output for data signals corresponding to at least the given bit location if at least one data signal for the given bit location differs from any remaining data signal for the given bit location;
attempting to read a word of the page of output;
determining whether output is disabled for at least the given bit location, wherein disabled output is indicative of failure of the memory device;
comparing a data value read from the memory array to a data pattern value written to the memory array; and
indicating failure of the memory device if the data value read from the memory array differs from the data pattern value written to the memory array regardless of whether any output is disabled.
95. The method of claim 94, further comprising:
repeating the method for each page of output of the memory device.
96. The method of claim 94, wherein further comprising:
repeating the method for each page of output of the memory device and attempting to read only one word of each page of output.